Listing Of Claims

Claims 1-51 (canceled)

52. (previously presented) A semiconductor component comprising:

a substrate comprising a plurality of tested semiconductor components including a plurality of component contacts and a plurality of integrated circuits in electrical communication with the component contacts, the components including at least one defective component; and

a metal layer on the substrate comprising a plurality of conductors in electrical communication with the component contacts configured to redistribute the component contacts into selected patterns, and to repair the defective component by connecting selected component contacts on the defective component with selected integrated circuits on the defective component.

53. (previously presented) The component of claim 52 wherein the components include a second defective component and the conductors are configured to electrically isolate the second defective component.

54. (previously presented) The component of claim 52 wherein the components include a second defective component and the conductors are configured to reconfigure the component contacts on the second defective component.

55. (previously presented) The component of claim 52 wherein the components include a second defective component and the conductors are configured to electrically connect multiple components in a cluster that excludes the second defective component.

56. (previously presented) A semiconductor component comprising:

a substrate comprising a plurality of tested components comprising a plurality of component contacts in a plurality of patterns;

the components including a plurality of good components and a defective component;

a metal layer on the substrate comprising a plurality of conductors configured to redistribute the patterns of the component contacts into selected patterns, and to electrically isolate the defective component on the substrate during burn-in testing of the good components.

57. (previously presented) The component of claim 56 further comprising a plurality of terminal contacts on the good components in the selected patterns in electrical communication with the conductors.

58. (previously presented) The component of claim 56 wherein the conductors are configured to electrically connect a plurality of good components in a cluster that excludes the defective component.

59. (previously presented) The component of claim 56 wherein the substrate comprises a semiconductor wafer, and the components comprise semiconductor dice or semiconductor packages.

60. (previously presented) A semiconductor component comprising:

a substrate comprising a plurality of tested semiconductor components comprising a plurality of integrated circuits and a plurality of component contacts in electrical communication with the integrated circuits, the components including at least one defective component;

a metal layer on the substrate comprising a plurality of conductors configured to redistribute patterns of the component contacts into selected patterns, and to reconfigure the component contacts on the defective component.

61. (previously presented) The component of claim 60 further comprising a plurality of terminal contacts on the components in the selected patterns in electrical communication with the conductors.

62. (previously presented) The component of claim 60 wherein the substrate comprises a semiconductor wafer or portion thereof and the components comprise dice or packages.

63. (previously presented) A test board for testing semiconductor components on a substrate including a plurality of good components and at least one defective component, each component having a plurality of component contacts, the test board comprising:

a plurality of first test sites comprising a plurality of contacts configured to electrically engage the component contacts on the good components on the substrate;

a plurality of second test sites configured to electrically isolate the defective component; and

a plurality of conductors configured to electrically connect the first test sites to a test circuitry and to electrically isolate the second test sites from the test circuitry.

64. (previously presented) The test board of claim 63 wherein the test board includes a patterned metal layer containing the conductors.

65. (previously presented) The test board of claim 63 wherein the test board is configured to perform a burn-in test and the second test sites are configured to electrically isolate the defective component during the burn-in test.

66. (previously presented) The test board of claim 63 wherein the substrate comprises a semiconductor wafer, and the components comprise dice or packages.

Claims 67-69 (Canceled)

70. (previously presented) A semiconductor component comprising:

a substrate comprising a plurality of tested semiconductor components including a plurality of good components and at least one defective component, each component comprising a plurality of contacts in first patterns, a plurality of integrated circuits in electrical communication with the contacts;

a plurality of terminal contacts on the components in ~~a~~ second patterns; and

a metal redistribution layer on the substrate comprising a plurality of conductors configured to redistribute the first patterns to the second patterns, and to electrically connect multiple components in a cluster that excludes the defective component.

71. (previously presented) The component of claim 60 wherein the terminal contacts comprise balls or bumps and the second patterns comprise ~~s~~ a grid arrays.

72. (previously presented) The component of claim 60 wherein the contacts comprise bond pads.

73. (previously presented) The component of claim 60 wherein the conductors fan out from the first patterns to the second patterns.

74. (previously presented) The component of claim 60 wherein the substrate comprises a semiconductor wafer.

75. (previously presented) The component of claim 60 further comprising a protective layer on the conductors having a plurality of openings for the terminal contacts.

76. (previously presented) The component of claim 60 wherein the components comprise semiconductor packages or dice.

77. (previously presented) The component of claim 60 wherein the components include a second defective component and the conductors are configured to repair, reconfigure or electrically isolate the second defective component.